TECH SPOTLIGHT

Thick High-Purity Silicon Coatings

Nilesh Gunda
Richard Cooke
*Santosh K. Jha**
*Suri A. Sastri**
Surmet Corporation
Burlington, Massachusetts

The prevention of wafer contamination from micro-particles (both physical and chemical) has become a major concern in the manufacture of devices in the semiconductor industry. Of particular importance is the control of metallic contamination, which can be fatal to semiconductor devices. Metallic contamination increases leakage current at P-N junctions, reduces oxide breakdown voltage, and shortens minority carrier lifetime in bulk silicon.

The risk of contamination is present in each step of the wafer manufacturing process. For example, during ion implantation, the silicon wafer is exposed to metallic contamination. During forward and backward sputtering, generation and transport of metallic contamination is possible from internal implanter surfaces. Graphite and aluminum are the two most common construction materials, but these are also contamination sources.

To prevent contamination, several coating methods have been applied to the surfaces of wafer manufacturing equipment. This article describes some common coating methods and their limitations. A new ultra-high purity (UHP) silicon CVD coating developed by Surmet is discussed and shown to be superior to existing technologies in many critical applications.

Conventional coatings

A common approach for reducing contaminants is to coat parts with a material that controls the level of contaminants and also provides resistance to erosion. Adhesion and surface finish must also be considered when selecting a coating for this purpose. The coating should be strongly adherent, and it should not require any further finishing.

Many coatings have been tried, including plasma-sprayed silicon and silicon carbide, sputter-deposited silicon, chemical vapor-deposited silicon, and bulk silicon carbide. However, all have limitations:

- Plasma sprayed silicon coatings are porous and can have large variation in grain size and surface finish. The surface finish may require post-spray finishing, which still cannot reduce high particle counts from these coatings. Purity is also difficult to control.
- Sputter-deposited silicon often has unacceptable levels of metal contaminants. Its low growth rate and high cost also make it unsuitable for the purpose.
- Chemical vapor-deposited silicon on aluminum is not possible because of the high deposition temperatures (550 to 600°C, 930 to 1110°F).
- Bulk CVD-grown silicon carbide has been considered as a replacement for aluminum in small machined parts for holding wafers. However, the mechanical properties of this material are inferior to those of aluminum, while the cost of machined parts is high.

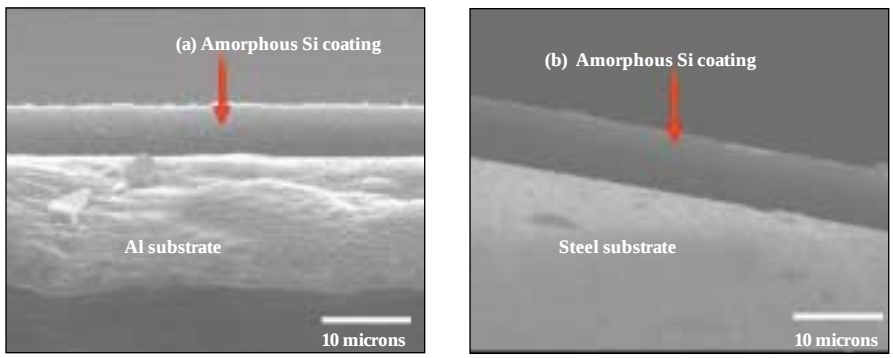

Fig. 1 — Cross-sectional SEM micrograph of ultra high pure silicon coating on (a) aluminum foil, and (b) steel blade. The coating is amorphous, microscopically homogeneous, and featureless.

UHP silicon coating

Surmet has recently developed a coating of ultra high-purity (UHP) silicon. The dust free UHP silicon is an engineered coating designed for high-performance wafer handling and pro-

Table 1 — Properties of UHP silicon coating

Substrates	**Metals, ceramics (AlN, Al_2O_3, quartz, YSZ, graphite, etc.) and polymers**
Structure	Amorphous, contains hydrogen.
Deposition temperature	<150°C, 300°F
Use temperature	–50 to 600°C (–58 to 1100°F)
Electrical resistivity	5×10^8 Ω-cm; (lower values are also possible)
Hardness	600 DPHN
Wear / abrasion resistance	Good
Corrosion resistance	Excellent resistance in aqueous, acidic, and alkaline environments.
Thickness	Uniform and conformal coating, ranging in thickness from a few nm to 150 µm (6 mils).
Substrate size and geometry	Any shape including complex, up to a size of 36 in. dia.
Applications	Particle reduction in semiconductor wafer processing; high precision optical mirrors for space and earth applications.
Key benefits	Ultra high purity, low residual stress, dense, hard, and micro-conformal; can be single-point diamond turned to optical finish.

**Member of ASM International*

Table 2 — PE-CVD silicon coating by GDMS analysis

Element	Concentration, ppm wt.	Element	Concentration, ppm wt.
B	<0.01	Fe	0.07
Na	0.05	Co	<0.005
Mg	<0.01	Ni	<0.01
Al	<0.5	Cu	<0.05
Ca	0.8	Zn	<0.1
Ti	<0.005	Zr	<0.01
V	<0.005	W	<0.05
Cr	<0.01	Pb	<0.05

cessing equipment in semiconductor industry applications. The dense, strongly adherent and conformal coating of silicon is deposited by means of a plasma-CVD process with deposition temperatures less than 150°C (300°F).

The coating reduces the levels of contaminating metals such as iron, copper, and chromium, which are found in the aluminum 6061 alloy, a common material in those applications. Reduction in the levels of aluminum and iron contamination on silicon wafers has been reported with these coatings. In addition, the dense coating provides an excellent, porosity-free surface with no post-deposition surface finish requirements.

The UHP silicon coating has a microscopically homogeneous structure with no visible features (Fig. 1). In addition, it has no sub-microscopic irregularities such as particles, voids, or growth lines. X-ray diffraction has shown the coating to be amorphous. The UHP silicon coating is compatible with a wide variety of substrates, including ceramics, metals, alloys, graphite, and polymers, in the thickness range from a few nanometers to over a hundred micrometers.

Complex shapes with shadowed cavities have been successfully coated. Many line-of-sight limitations such as those encountered in conventional physical vapor deposition processes have been overcome. Table 1 highlights the properties.

Excellent adhesion and conformity to the substrate lead to a totally dust free, smooth surface. The fully dense, well-adhered coating does not trap or generate particles. It has ultra high purity (99.999%), with metallic impurity content reduced to below one part per million. This is illustrated in Table 2, which lists the concentration of various elements measured by glow-discharge mass spectrometry analysis.

UHP silicon coatings are applied to exposed metal surfaces inside wafer processing chambers to prevent metallic contamination during processing. Fig. 2 shows an aluminum part from a wafer processing chamber coated with 25 µm thick UHP silicon. The coating can also be applied on inside surfaces of the entire processing chamber. Fig. 3 shows a portion of a coated process chamber.

Fig. 2 — An aluminum alloy 6061 part coated with ultra high purity silicon (99.999%). The coating thickness is about 25 µm.

Fig. 3 — UHP silicon coating (99.999 %) on internal surface of a process chamber. The coating is uniform and micro-conformal, with a clean and shining surface.

UHP silicon is proving to be an enabling technology for wafer processing and other high technology environments. Microparticle reduction, which is so critical in semiconductor industry, is being achieved during both physical and chemical processing of wafers for device fabrication. ■

For more information: Dr. Ramas Raman and Rick Cooke, Surmet Corp., 33 B Street, Burlington, MA 01803; tel: 781/272-3969; fax: 781/ 272-4521; Web site: www.surmet.com.